

# A 12.5Gbps Analog Timing Recovery System for PRML Optical Receivers

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**Abstract** — This paper describes a timing recovery system (TRS) based on an analog approximation of the minimum mean squared error (MMSE) algorithm. The TRS has been fabricated in a 0.18 $\mu$ m, 150GHz SiGe BiCMOS process as part of a high performance Class-2 Partial Response Maximum Likelihood (PRML) dispersion tolerant optical receiver. This decision directed clock recovery architecture was implemented for the (1+D)<sup>2</sup> partial response polynomial. The TRS supports all XFI data rates [9.95, 11.09]Gbps and has been verified up to 12.5Gbps. The TRS is functional at OSNRs as low as 11dB and has been verified in the full PRML receiver at a BER of 10<sup>-4</sup> over 400km of uncompensated single mode fiber (SMF). It dissipates 372mW from a dual 3.3V and 1.8V supply and complies with or exceeds all XFI receiver Jitter specifications for Telecom (SONET OC-192 and G.709 “OTU-2”) and Datacom (Ethernet 802.3ae or Fiber Channel).

**Index Terms** — CDR, MLSE, partial response signaling, PLL, PRML, PRS, timing recovery.

## I. INTRODUCTION

Maximum-likelihood sequence estimation (MLSE) has been shown to be a powerful technique for electronic compensation of both chromatic and polarization mode dispersion [3]-[4]. For the first time, to our knowledge, we propose a new kind of receiver based on the principles of partial-response maximum likelihood equalization techniques implemented in the analog signal domain [5]. This paper will describe the timing recovery system of the receiver.

Fig. 1 shows a simplified block diagram of the TRS. The received NRZ data is first passed through an AGC controlled VGA and equalized with a gm-C continuous-time-filter (CTF). The CTF approximates a linear phase or constant group delay response up to approximately 1.2 times its programmable cutoff frequency which is optimized along with the Finite-Impulse-Response (FIR) filter transfer function for equalization of the input signal to the target partial response polynomial, (1+D)<sup>2</sup>. The primary function of the TRS is to provide the FIR filter with the optimal clock phase for proper equalization. Phase information for the data samples is contained in the difference between the samples and their ideal value [1].

The TRS decision directed phase detector (DDPD) employs the MMSE algorithm to achieve this.

## II. TIMING RECOVERY ARCHITECTURE

The architecture consists of three components: a time-interleaved DDPD, a frequency lock loop, and a digital controller or lock detect block (LD). The frequency lock loop is a traditional phase-frequency detector type-2 charge-pump PLL. The initial step in the frequency acquisition process is a coarse calibration of the multiple band differentially tuned LC-VCO. The VCO has a 4-bit coarse tuning control giving the LC-Tank sixteen distinct frequency bands. During coarse tuning, the VCO is set to the center frequency of each band. Then, the LD sequentially transverses each zone comparing the center frequency (divided by 64) of each band to the reference frequency and chooses the zone with the smallest frequency offset. Frequency acquisition is completed by the PLL before switching control to the DDPD.

The phase acquisition process can be understood by referring to the block diagram in Fig. 1. The FIR interleaves the full-rate CTF output into two partial response data vectors; the 0° phase  $y_k(A)$  vector and the 180° phase  $y_k(B)$  vector. In contrast to standard binary phase detection, the discrete time analog PRS has five possible levels, for our Class-2 target polynomial  $(1 + D)^2$ , these levels are:  $\{0, \pm 1, \pm 2\}$ . At sample time k, the DDPD uses an ideal PRS generator, the 5-level quantizer, or slicer shown in Fig. 1, to produce an ideal sample  $y_k^*$  for each sample  $y_k$ . An error signal is generated and delayed ( $e_{k-1} = y_k^* - y_{k-1}$ ) between the ideal and actual sample. This error signal, (along with other PLL loop parameters), defines the magnitude of the analog phase adjustment. The polarity of the phase adjustment is determined by the slope ( $M_k = y_k - y_{k-2}$ ) at each sample point of the discrete time analog PRS. The product of the slope and amplitude error produces the phase error ( $\Phi_k$ ) for the sample data at time k. The amplitude error is computed in the opposite phase interleave with respect to its slope calculation. The voltage domain phase errors from both phases are summed

together by a differential transconductor (Gm) which drives the loop filter and VCO.

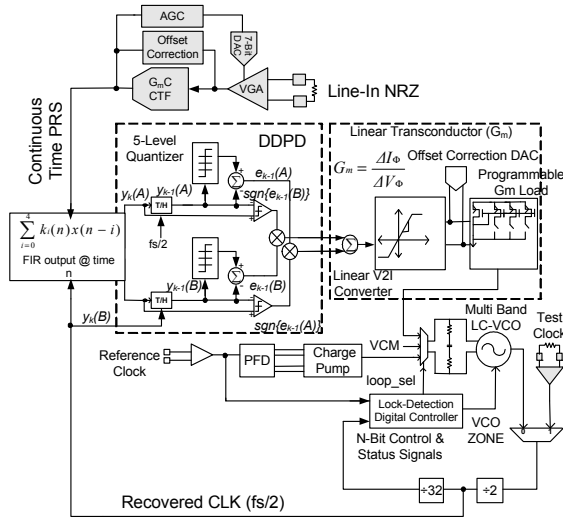


Fig. 1. Timing Recovery Functional Diagram.

### III. MMSE BASED TIMING RECOVERY

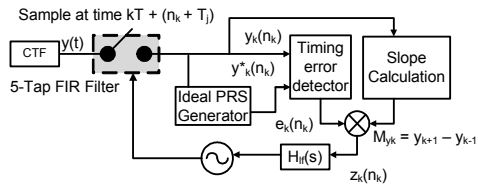


Fig. 2. MMSE timing recovery conceptual diagram.

Fig. 2 depicts the basic concept of the MMSE timing recovery algorithm. MMSE based timing recovery is the application of the Least-Mean-Square (LMS) adaptation technique to acquire phase in a sampled data clock recovery system [2]. Simply stated, the timing information is obtained as the instantaneous gradient, with respect to phase; of an error signal that is proportional to the phase. The received NRZ data is passed through the CTF whose impulse response is such that the output  $y(t)$ , when sampled at the appropriate phase, yields a sequence that corresponds to the target polynomial. The MMSE input signal  $y(t)$  is sampled at time  $(kT + (n_k + T_j))$ ; where  $T$  is the sample interval,  $n_k$  represents the optimal timing offset for the optimal sample phase of sample  $k$ , and  $T_j$  is timing jitter. To arrive at this optimal timing, the phase error of the loop is derived in magnitude by the amplitude error  $e_k$  which is the difference between the equalized sample  $y_k$  and the quantized or ideal estimated value  $y_k^*$ , as shown in (1).

$$e_k = y_k^* - y_k \quad (1)$$

$$MSE = E\{e_k^2\} = \int_{-\infty}^{\infty} e_k^2 PDF(y_k) dy_k \quad (2)$$

$$\frac{de_k^2}{dn_k} = -2e_k(n_k) \left[ \frac{d}{dt} y(t) \right]_{t=kT+n_k} \quad (3)$$

Modulation of the sample phase will produce a corresponding change in  $y_k$ ; therefore the minimum of the MSE (2) is found by setting the derivative with respect to the sampling time of (2) to zero and setting the timing jitter to zero. The minimum occurs when the product of the amplitude error for sample  $k$  and the slope of the sample at time  $k$  is equal to zero. So, if the phase of the VCO is modulated with (4)

$$z_k = e_k \times (y_{k+1} - y_{k-1}), \quad (4)$$

the expected squared error will be minimized by adjusting the sample timing phase in the data path feedback loop.

### IV. PHASE DETECTOR FUNCTIONALITY

The interleave topology of the fully differential DDPD is shown in Fig. 3. The sample under measurement ( $y_n$ ) is sent to two track and hold based current mode logic (CML) processing paths. One path computes the amplitude error (partial response target error), the other determines the instantaneous slope of the sample whose target error is being computed in the opposite interleave.

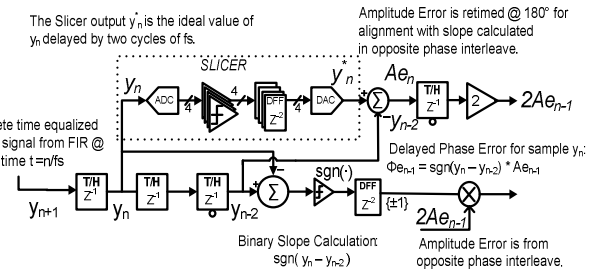


Fig. 3. DDPD interleave architecture.

with  $y_n$ , a data symbol under timing error measurement. The top half circuitry will calculate the amplitude error  $Ae_n$  by sending  $y_n$  through the slicer. The slicer is a 5-level quantizer, whose digital output words are concatenated to drive a reconstruction DAC. The output of the slicer is the best estimate of the input sample to the target polynomial. Ideal equalization to the  $(D^2 + 2D + 1)$  target polynomial yields five discrete equally spaced signal levels:  $\{0, \pm 1, \pm 2\}$  the slicer will map  $y_n$  to one of these signal levels. The difference between the quantized value ( $y_n^*$ ) and the received sample ( $y_n$ ) is computed and retimed in phase with its slope. The delayed error  $Ae_{n-1}$  is then sent to a 6.0

dB linear amplifier which drives the analog input of a saturated multiplier. The digital input to the multiplier is the sign of the slope  $\{\pm 1\}$ . The difference between the next sample and the previous sample is computed and quantified with a signed comparator. The product of the amplitude error and the sign of the slope form the phase error for one phase of the PRS. The outputs of both interleaves are summed together in the transconductor to produce a continuous time differential phase error.

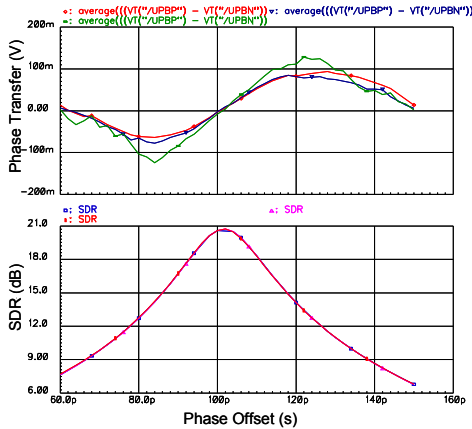


Fig. 4. DDPD phase transfer characteristic, PTC, (top) and signal to distortion ratio, SDR, (bottom) as a function of phase offset for model (ideal), schematic, and layout parasitic extracted netlist.

In addition to the traditional specifications for clock and data recovery systems (i.e Jitter Tolerance, Jitter Transfer, etc.) our MMSE based interleaved analog architecture must satisfy a strict linearity specification. The linearity metric is a measure of the amount of “mis-equalization” the TRS introduces in the timing recovery process. The “mis-equalization” is a deviation from the ideal sample point, resulting in a static phase offset, which causes the system to lock to some point less than the maximum SDR value.

Fig. 4 shows the PTC and SDR vs. phase offset for 11.1Gbps PRBS-7 data across a span of 160km of SMF under nominal conditions. The MMSE should be zero at the maximum SDR. The theoretical maximum SDR possible at the PRML detector input for this input signal is  $\sim 20.6$ dB (Fig. 4 bottom) and Fig. 4 (top) shows that our circuit LMS implementation finds the minimum at 440fs offset with respect to the mathematical model. This 440fs static phase offset results in less than a 0.2 dB penalty in SDR. Simulations show a worst-case, over PVT and offset, of 780fs of static phase offset.

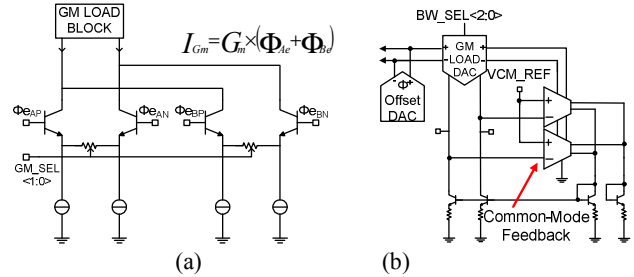


Fig. 5. (a) The Linear Transconductor input and interleave summing connection and (b) the load block.

## V. Transconductor and Loop Dynamics

The GM continuously sums the interleaved voltage signals in the current domain via two independent fully differential voltage-to-current converters sharing a common load, as shown in Fig. 5. The PMOS current mirror load composes the top half or current “source” of the GM output stage. The transconductance of the GM is controlled digitally by emitter degeneration. A 2-bit binary control is converted into a 1-of-n code, where the three resulting bits are used to selectively shunt unit resistance segments. The programmable degeneration defines the overall input voltage versus output current linearity range and sets the transconductance.

Since the phase transfer of the DDPD is a linear function of phase error, this LMS based phase-detector is seen as a linear phase detector in the PLL loop dynamics. For this to remain valid the GM also needs to be a linear function of its input phase-error. Therefore, a 2-bit emitter degeneration DAC gives us 4 distinct loop bandwidth settings covering a 4X range. To further enhance programmability, a 3-bit binary DAC scales the final output current and final transconductance for each of the degeneration settings. The GM output current is divided into eighths, one eighth is sent directly to the loop-filter, the remaining 87.5% of  $I_{GM}$  is linearly distributed over the 3-bit binary DAC. An additional 7-bit binary current steering DAC is also implemented to correct asymmetry or systematic offset that may be present in the timing error data-path. The digitally controlled emitter degeneration (2-bits) defines the overall input voltage vs. output current linearity range and sets the initial transconductance. The 3-bit DAC only scales the final output current and, hence the final transconductance, for a given degeneration setting. This permits another degree of freedom,

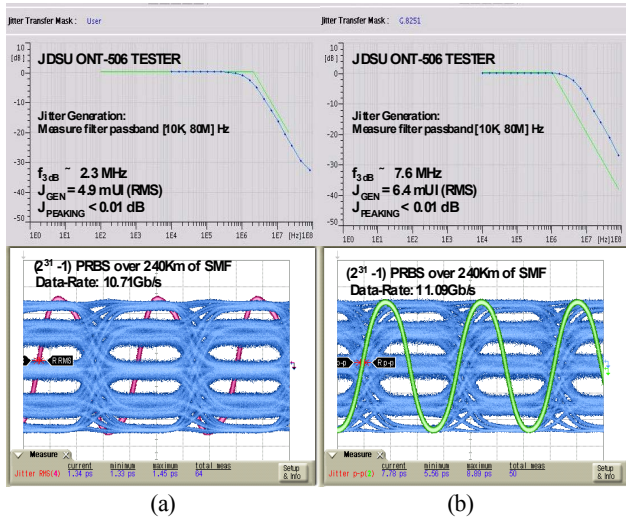


Fig. 6. Jitter Transfer response (top) and Recovered Clock & FIR eye for two different bandwidth settings (a) 2.3MHz and (b) 7.6MHz.

since the linearity range can now be set independently of the overall transconductance. It is quite beneficial, since the gain that was traded for linearity can now be recovered and returned.

## VI. MEASUREMENT RESULTS

The TRS along with the analog Viterbi Decoder comprise the clock and data recovery unit of a fully integrated XFI receiver. The recovered clock is accessible via a high-speed linear Test-Point MUX and buffer. The Jitter Tolerance was verified for a 240km SMF span at 11.09Gbps with the TRS programmed to a bandwidth of 8.0MHz. The actual measured bandwidth for this setting was  $\sim 7.6$ MHz. A JDSU ONT-506 Tester was used for this measurement and the results along with the SONET Jitter Tolerance mask are shown in Fig. 7(a). The compliance is normalized for a BER of  $10^{-6}$ . The top of Fig. 6(a), shows the measured Jitter Transfer, Peaking, and Jitter Generation for this measurement:  $f_{3dB} \sim 7.6$ MHz,  $J_{GEN} = 6.4mUI_{rms}$ , and the Jitter Peaking is  $< 0.01$  dB. The recovered clock and one phase of the FIR output or Viterbi input are shown in the lower half. Fig. 6(b) shows the results for the same Jitter metrics at 10.71Gbps for a lower loop bandwidth setting. The loop bandwidth was set to 3.6MHz (measured  $\sim 2.3$ MHz) and the measured Jitter Generation is  $4.9mUI_{rms}$ . Fig. 7(b)-(d) shows the VGA input, one phase of the FIR, and the recovered clock and data for a PRBS ( $2^{31}-1$ ) input signal over 320km of SMF at 10.71Gbps Fig. The BER was  $> 10^{-5}$  and the input OSNR was 22dB.

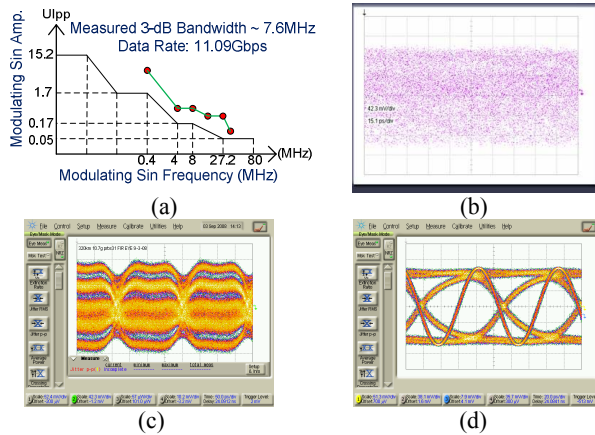


Fig. 7. (a) Measured jitter tolerance vs. mask, (b) 320km input eye, (c) 320km FIR output or Viterbi input, (d) 320km recovered clock and NRZ data.

## VII. CONCLUSION

A fully differential time-interleaved high-speed analog timing recovery system for a high performance PRML Class-2 dispersion tolerant optical receiver has been implemented in  $0.18\mu m$  SiGe BiCMOS. The TRS circuit employs a type-2 charge pump PLL for frequency acquisition, and a decision-directed LMS algorithm for phase acquisition. The TRS architecture was implemented for the  $D^2 + 2D + I$  PRS, but is suitable for any partial-response polynomial. The circuit supports all XFI data rates [9.95, 11.09]Gbps, and data-rates as high as 12.5 Gbps. The TRS provides SONET compliant jitter generation, tolerance and transfer and dissipates 372mW from a dual 3.3-V and 1.8-V supply.

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