A 50 dB Dynamic Range, 11.3 GSPS, Programmable Finite Impulse Response (FIR) Equalizer in 0.18µm SiGe BiCMOS Technology for High Speed Electronic Dispersion Compensation (EDC) Applications

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Abstract — A Finite Impulse Response (FIR) equalizer utilizing 0.18µm SiGe BiCMOS provides unparalleled performance as a building block for analog Electronic Dispersion Compensation (EDC) applications. A new track-and-hold (T/H) topology improves on the existing performance limitations of the Switched Emitter Follower (SEF) architecture. The new T/H achieves extended dynamic range, for higher input bandwidths, at lower power consumption. The FIR circuit has been included as a building block in the implementation of an analog EDC IC that is the world's first demonstration of 10.7 Gbit / s error free operation over 400 km of uncompensated SMF fiber.

Index Terms — Programmable filters, sample and hold circuits, optical communications, multiplying circuits, low pass filters.

I. Introduction

Fiber optic signals transmitted over long lengths of single mode fiber (> 80km) suffer from various forms of dispersion. This translates into signal distortion in the electrical domain. Equalizers such as a FIR filter is used to transform the severely distorted NRZ data into a predictable pre-defined target signal that allows for robust clock and data recovery. There are several key features of the FIR in support of the performance needed for this application. An improved wideband track-and-hold (T/H) topology achieves high speed and resolution at low power levels. A wideband, fast settling current summing node for the FIR tap coefficients supports a high signal dynamic range (SDR) for the signal path. The resultant performance of the FIR, in conjunction with the performance of other blocks on the chip, allows the overall EDC IC to obtain unprecedented bit-error-rate (BER) performance over long haul fiber networks.

II. FIR Description

Figure 1 shows an overall block diagram of the functionality of the 5 tap FIR. On the EDC IC, the input variable gain amplifier (VGA) and CTF precede the FIR, and these circuits provide gain and equalization of the input signal so the optimum signal swing is presented to the FIR. The FIR provides further equalization of the

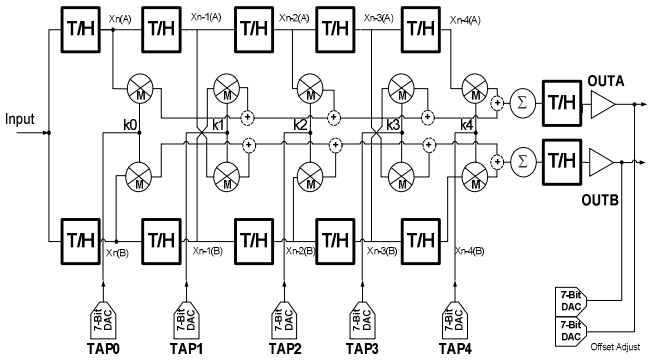

Fig. 1. Interleaved 5 Tap FIR Architecture.

signal. For a 10 Gbit / second application, with an interleaved T/H structure for the FIR, each T/H resultantly operates at 5 GSPS, with the sampling clocks 180 degrees out of phase for each T/H bank. Each tap coefficient is generated through a DAC, and a Gilbert cell is used to multiply the signal by the digitally programmed tap weight. The outputs of the Gilbert cells are current mode signals that are summed together to drive the output T/Hs. Each of the interleaved outputs has a digitally controlled offset voltage to optimize the received signal as a function of the optical reach. In order for proper operation of the

FIR at high sample rates, the clock skew between the first T/Hs must be controlled to < 1ps. This requires careful layout considerations and extracted simulations.

III. New T/H Topology

A key enabling circuit for the FIR is a new T/H circuit topology. The standard switched emitter follower (SEF) based T/H architecture [1] has been enhanced by the addition of an isolation buffer stage from the output of the G_M stage to the SEF input. Figure 2 is the schematic of the

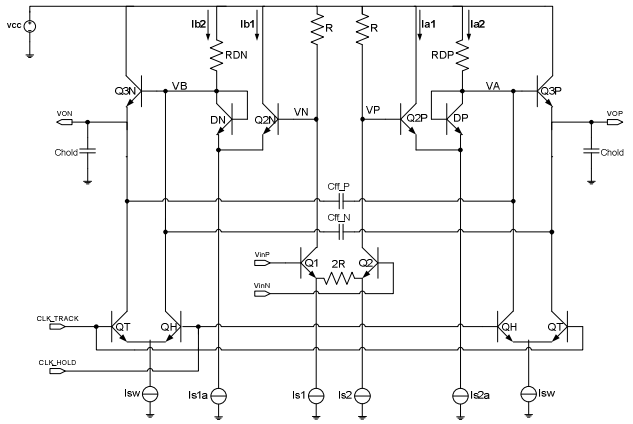

Fig. 2. T/H Architecture with Isolation Buffer.

improved T/H design [2]. The isolation buffer consists of transistors Q2P, Q2N, DP, and DN and resistors RDP and RDN. In track mode, the buffer provides a zero volt level shift, and the output impedance is significantly lower than previous implementations, where the G_M stage, with the high output impedance, provides a poor drive capability at high frequencies. The low output impedance feature of the buffer in the new T/H provides enhanced drive capability for the SEF and feed-forward capacitors, which results in improved track mode acquisition settling time. This is accomplished without the need for increased power dissipation. In hold mode, the transistors DP and DN are reverse-biased due to the differential pair current Isw into RDP and RDN. The resultant hold mode isolation provides reduced feed-through as compared to the previous approach. This is a consequence of the reverse-bias voltage on the CJE of the SEF transistors Q3P and Q3N. The differential T/H circuit dissipates 30 mW on a 3.3V power supply. The performance of the T/H was simulated under various conditions to determine the anticipated dynamic range. The simulated track mode bandwidth (BW) of the T/H is 22 GHz. The third harmonic distortion (HD_3) for the differential T/H was simulated under Nyquist conditions, at 5 GSPS and 10 GSPS, with 1V peak-to-peak (pp) input signal. The simulated sampled mode HD_3 performance was 54 dBc and 43 dBc, respectively, assuming no mismatch between the (+) and (-) channels of the T/H.

Ref. No.	Fsample [GHz]	Fin [GHz]	Input [Vpp]	ENOB [bits]	BW [GHz]	Supply [V]	Power [mW]	Process / FT
[3]	10.0	1.0	1.0	6.8	2.7	3.3	70.0	SiGe/200
[4]	12.1	1.5	1.0	8.0	5.5	3.5	700.0	SiGe/200
[5]	1.2	0.6	1.0	8.0	2.0	+2.0/-0.5	460.0	Si/25
[6]	4.0	8.0	0.6	6.0	10.0	5.2	550.0	SiGe/45
[7]	10.0	3.0	2.0	8.3	4.8	5.0	587.5	SiGe/200
This work	10.0 (*)	5.0	0.9	7.8	22.0	3.3	30.0	SiGe/120

Fig. 3. Comparison of Published Si / SiGe High Speed T/Hs with this work.

(*) Interleaved Architecture

IV. Gilbert Summing Juction

Figure 4 is the schematic of the Gilbert cells that are driven by the output of the T/Hs in Figure 2. The digitally controlled tap coefficient scales the output signal from each T/H. The output of each Gilbert cell drives a transconductance amplifier. The cascodes QC1 and QC2 sum the output currents of the transconductance amplifiers, and the output drive the final T/Hs in Figure 1.

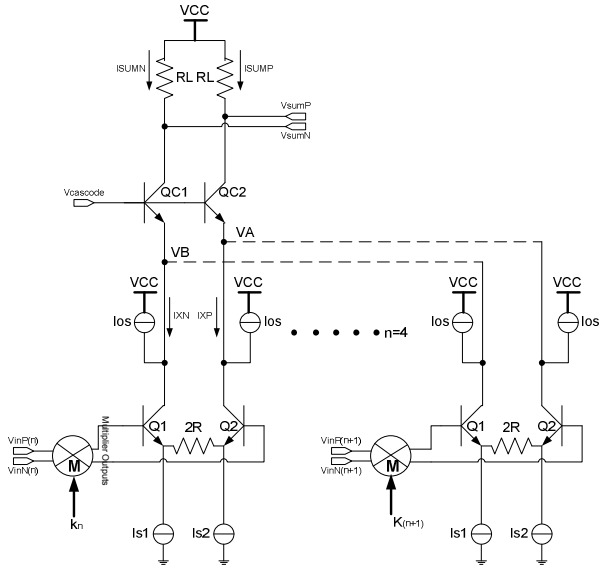

Fig. 4. Block Diagram of the FIR Summing Node.

V. Test Results

Figure 5 shows the test set-up for the characterization of the FIR. The feed-through of the VGA / CTF / FIR is measured with the tap coefficients set so that all the Gilbert cells are balanced, and the FIR input is isolated from the FIR output. The input data from the signal generator is 11.1 Gbit / second PRBS-31 NRZ signal, with a coherent tone at 0 dBm. The VGA / CTF provides gain of the input signal to present a full-scale differential signal of +4 dBm to the FIR. The measurement of the coherent tone at the test buffer is -40.8 dBm. The test buffer differential-to-single-ended gain is 0.45 (-6.9 dB), which produces -33.9 dBm at the FIR output. The noise floor of the T/H block was simulated and correlated to measurement. The simulated sampled mode RMS noise for a single T/H is 3.2 mV at the measured junction temperature. A high speed sampling oscilloscope, referred to here as the DCA, is used to measure the RMS noise of the output T/H in Figure 1 with all the FIR tap coefficients set to zero. This allows the dominant noise source of the signal path to be the output T/H. The measured RMS noise must be referred back to the T/H through the gain of the test buffer. The measured RMS noise is 1.7 mV at the single- ended output of the test buffer. The test buffer gain is 0.45, which results in a T/H differential noise = 3.4 mV, which agrees well with simulation. The FIR tap delay, from tap #1 output to tap #5 output, is measured to be 401.9 ps, compared to an ideal value of 400 ps. The tap-to-tap delay is approximately 100 ps (i.e., the symbol period for a 10 Gbit /s second signal). The FIR gain is measured at each of the 5 taps, for all of the 7 bit DAC codes, and from the measured transfer function in Figure 5, it can be seen that the FIR tap gain is a linear function of the DAC codes. Figure 6 demonstrates the functionality

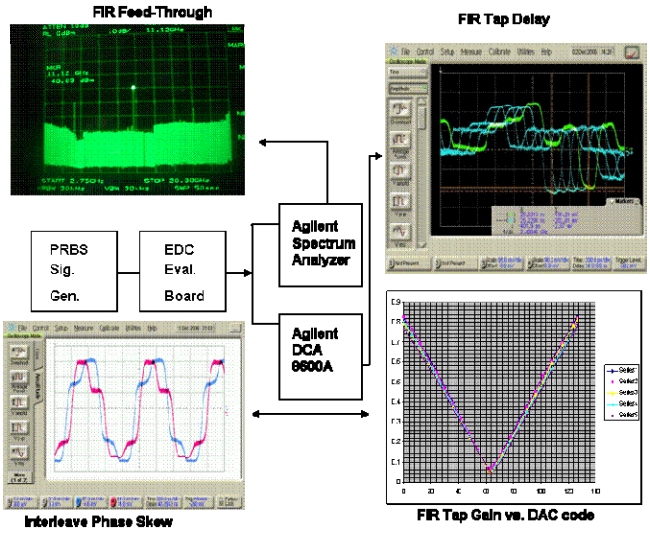

Fig. 5. Test Measurement Set-Up.

of the FIR with the tap coefficients programmed to configure the FIR as a low pass filter. The FIR coefficients, AC transfer function, group delay, and time domain waveforms were verified through simulation. For the measurement, the input to the FIR is the output of the

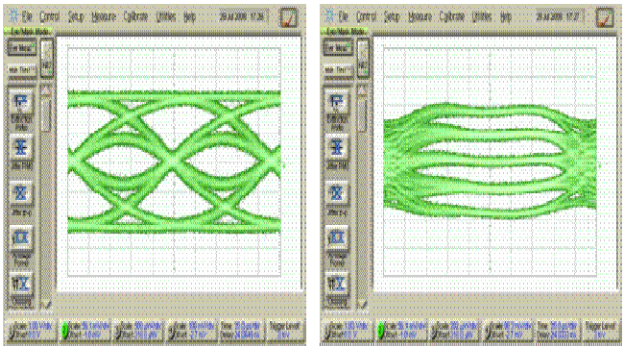

Fig. 6. FIR 3 level input signal and 5 level output signal.

CTF on the EDC IC. The CTF produces a 3-level PRBS signal @ 10 Gbit / second. The target response is a 5-level signal obtained from the following transfer function:

$$H(z^{-1}) = 0.5 + z^{-1} + 0.5z^{-2} \quad (1)$$

where z^{-1} represents a symbol delay. The FIR time domain measured response closely matches the ideal target. The DCA is used to capture the time domain waveforms. Figure 7 is a die photo of the EDC IC, and the chip location of the FIR is highlighted. The FIR performance enables unprecedented dispersion compensation for long haul fiber optics networks.

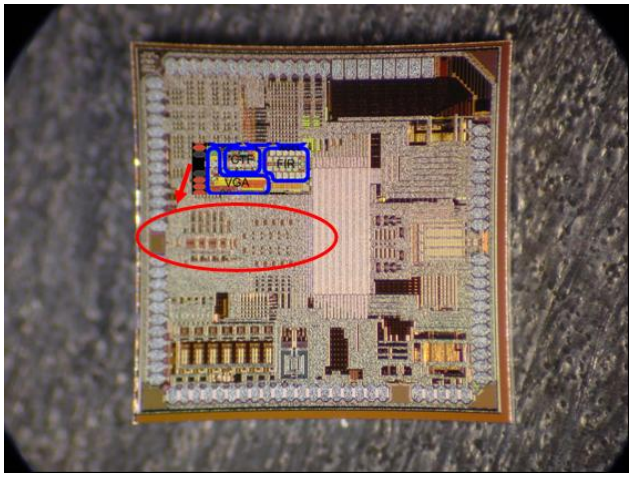

Fig. 7. EDC IC Die Photo and Chip Location of VGA / CTF / FIR Circuitry.

V. Conclusion

This paper presents a 5 GSPS, interleaved T/H based FIR architecture with state-of-the-art performance. This performance is enabled through the development of an improved T/H circuit topology. This new T/H achieves high dynamic range and high bandwidth with low DC power consumption. The FIR circuit has been used as a building block in the implementation of an EDC integrated circuit. The analog EDC IC is the world's first demonstration of 10.7 Gbit / s error free operation over 400 km of uncompensated SMF fiber [8].

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